NTNU – Trondheim
Norwegian University of
Science and Technology

Department of Physics

Examination paper for TFY4185 Measurement Technique/ Måleteknikk

Academic contact during examination: Patrick Espy

Phone: +47 41 38 65 78

Examination date: 15 August 2015

Examination time (from-to): 09:00 – 13:00

Permitted examination support material:

Single or Bi-lingual dictionary permitted
All calculators permitted
1 side of an A5 sheet with printed or handwritten formulas permitted

Other information:

Language: English

Number of pages: 9 + cover

Number of pages enclosed: 10

Checked by:

_____

Date Signature

The Norwegian University of Science and Technology Department of Physics
ENGLISH

Contact person:
Name: Patrick Espy
Tel: +47 73 55 10 95 (office) or
+47 41 38 65 78 (mobile)

EXAM IN TFY 4185 Measurement Technique/Måleteknikk

Augut 2015
Time: 09:00-13:00

Number of pages: 14

Permitted aids: 1) Dictionary (ordinary or bi-lingual)
2) All calculators
3) 1 side of an A5 sheet with printed or handwritten formulas permitted

You can answer in either Norwegian or English. The weight for each multiple-choice question is 4%, the weight for each calculation problem is given in parenthesizes.

The solutions to the multiple choice-questions are given in a light red colour. I have given the justification for the solution, but will only grade the multiple-choice answer.

Multiple Choice Questions-1 (40% total).

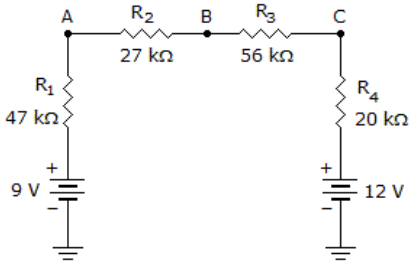
There is only **one** correct answer so you must **choose the best answer**. Answer A, B, C… (Capital letters). Correct answers give +4; incorrect or blank answers give 0.

Write the answers for the multiple choice questions **on the answer sheet you turn in** using a table similar to the following:

Question	1	2	3	4	5	6	7	8	9	10
Answer	**A**	**C**	**D**	**B**	**A**	**C**	**C**	**D**	**B**	**B**

Design a logic circuit to take three inputs – A, B and C – and produce a single output X, such that X is true if, and only if, precisely two of its inputs are true.

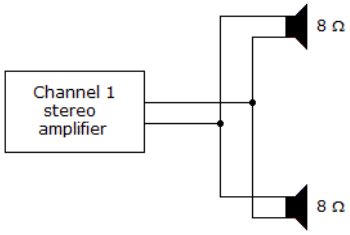
1. **Calculate the voltage at point B in the following circuit:**



A) 10.5 V B) 0.9 V C) 2.6 V D) 3.0 V

Current will flow from high to low potential, or 12 to 9 V. This potential difference will drive a current across the series resistors of (12-9)V / (R_1+R_2+R_3+R_4). So I = 3 V/150 kΩ = 20 μA. Starting at 12 V, the voltage drops to 12V-I*(R_4+R_3) = 10.5V at B. Or one could say 9 V + I*(R1+R2) = 10.5 V.

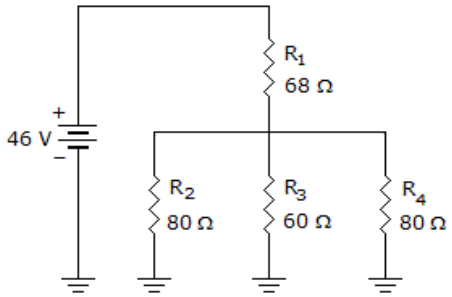
2. **In the following circuit, Channel 1 of the stereo amplifier outputs 12 V to the speakers. How much total current is the amplifier providing to the speakers?**



A) 0.75 A B) 1.5 A **C) 3.0 A** D) Not enough information given

The two speakers are in parallel presenting a net load of R_L=(8Ω·8Ω)/(8Ω+8Ω) =4Ω. The 12 V across this load will produce a current I = 12 V/ 4Ω = 3A.

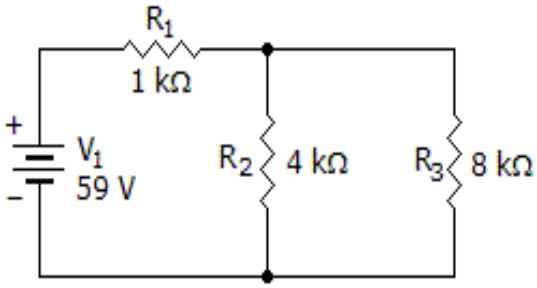
3. How much voltage is dropped across R3 in the given circuit?



A) 46 V B) 21 V C) 34 V **D) 12V**

Take R_2, R_3 and R_4 in parallel as $1/R_t=1/R_2+1/R_3+1/R_4 = 0.042\Omega^{-1} \Rightarrow R_t=24\Omega$. Now in the voltage divider of R_1 and R_t, the voltage across R_t is $V_{Rt}= V*R_t/(R_1+R_t) = 46V*24\Omega/(68\Omega+24\Omega) = 12V$

4. What is the power dissipated by R1, R2, and R3?



A) P1 = 0.13 W, P2 = 0.26 W, P3 = 0.12 W

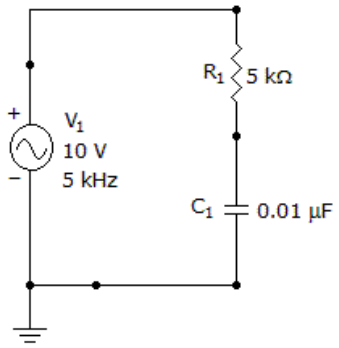
B) P1 = 0.26 W, P2 = 0.52 W, P3 = 0.23 W

C) P1 = 0.52 W, P2 = 0.92 W, P3 = 0.46 W

D) P1 = 1.04 W, P2 = 1.84 W, P3 = 0.92 W

The total current is flowing across R_1 in series with the parallel pair R_2 and R_3 that have an equivalent resistance $R_{//} = (R_2 \cdot R_3)/(R_2+R_3)$. So the total resistance is R_T given by 1 kΩ + (4 kΩ ·8 kΩ) / (4 kΩ + 8 kΩ), or R_T = 3.67 kΩ. The total current is $I=V_1/R_T$, or I = 59V/3.67 kΩ = 16.1 mA. This current flows through R_1 causing the supply voltage to drop $I \cdot R_1$ volts to V_2= 59V - 0.0161A·1000 Ω = 42.9 V. This voltage across will create a current I_2=42.9 V/R_2, and a current I_3=42.9V/R_3 across R_3. Substituting in values, we have I_1= 16.1 mA, I_2= 10.7 mA and I_3 = 5.3 mA. Therefore the power dissipated in the three resistors = $I^2R \Rightarrow$P1 = (16.1 mA)^2·1 kΩ = 0.26W, P2=($I_2^2 \cdot R_2$) = V_2^2/R_2 = 0.46 W, and P3=($I_3^2 \cdot R_3$) = V_2^2/R_3 = 0.23 W. While the exact answer is not present, the closest (and therefore the best) answer is B (all other answers differing by factors of two from the calculated values).

5. What is the total impedance of the following circuit?



A) 5928 Ω

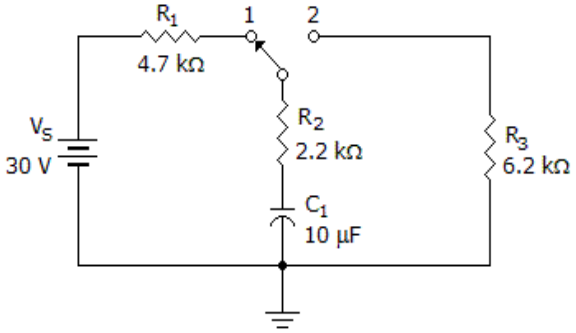
B) 8183 Ω

C) 20 kΩ

D) 126 kΩ

The impedance is $Z = R_1 - j/(\omega C)$, where $\omega = 2\pi * f = 31416$ r/s. This gives $Z = 5000 - j(3183)$ Ω. The magnitude of the impedance is $|Z| = \text{sqrt}((5000)^2 + (-3183)^2) = 5928$ Ω.

6. In the following circuit, what with the voltage be across R3 at a time t = 25 ms after the switch is moved to position 2?

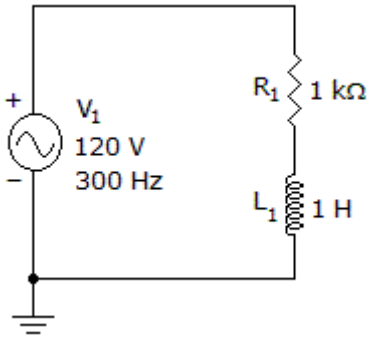


A) 2.7 V B) 5.8 V **C) 16.4 V** D) 22.3 V E) 30.0 V

When the capacitor is fully charged with the switch in position-1, the current stops flowing in the circuit. At this point, the voltage across the capacitor is Vs. When the switch is moved to positon 2, this initial voltage on the capacitor begins to discharge through R2 and R3 with a time constant

$T = (R2+R3) = 10\text{x}10^{-6}$ F*(2200+6200) Ω = 84 ms. Thus, 25 ms into the discharge cycle the voltage in the circuit is V = Vs*exp(-25/84) = 22.3 V. The current in the system at this time is I = V/(R2+R3) = 22.3V/(2200+6200) Ω = 2.65 mA, and the voltage drop across R3 will be I*R3 = 2.65 mA * 6.2 kΩ = 16.44 V. Note that since the initial voltage only depends upon Vs and not on the resistances in the charging circuit, this is the same in the discharging circuit.

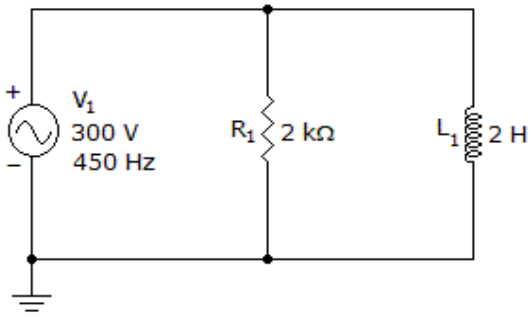
7. Find the voltage across the resistor (V_R) and the voltage across the inductor (V_L) in the following circuit?



A) V_R = 41.6 V, V_L = 78.4 V
B) V_R = 48 V, V_L = 110 V
C) V_R = 56 V, V_L = 106 V
D) V_R = 60 V, V_L = 60 V

The frequency of 300 Hz corresponds to an angular frequency of 1885 r/s. The resistance has impedance of 1000 + j(0) Ω, while the inductor impedance is $Z_L = j\omega L = j(1885r/s*1H)=j(1885)\Omega$. The magnitude of the impedance is therefore $|Z| = sqrt(R^2+Z_L^2) = 2134\ \Omega$. The current through the system is $I=V/|Z| = 120V/2134\Omega = 0.056$ A. Thus the voltage across the resistor, $V_R= I*|R| = 56$ V, and across the inductor, $V_L = I*|Z_L| = 106$ V.

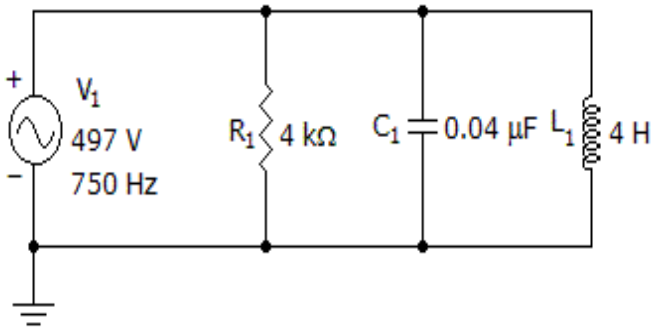
8. Find the currents through R_1 and L_1 (I_R and I_L), and the total current, I_T.



A) I_R = 50 mA, I_L = 109 mA, I_T = 159 mA
B) I_R = 150 mA, I_L = 9 mA, I_T = 159 mA
C) I_R = 50 mA, I_L = 151 mA, I_T = 201 mA
D) I_R = 150 mA, I_L = 53 mA, I_T = 159 mA

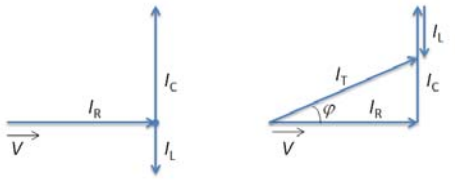
The voltage across R_1 and L_1 is the same: V_1=300V. This voltage will cause a current $I_R = V_1/R_1 = 300\ V/2000\ \Omega = 150$ mA to flow in R_1. The reactance of the inductor is $X_L=2\cdot\pi\cdot f\cdot L=\omega\cdot L = 2\cdot\pi\cdot 450Hz\cdot 2H = 5655\ \Omega$. The voltage V_1 across this reactance will cause a current $I_L = V_1/X_L = 300\ V/5655\ \Omega = 53$ mA to flow in the inductor. However, since the current and voltage will be in phase in the resistor but out of phase in the inductor, the two currents need to be summed as vectors with a magnitude $I_T = (I_R^2 + I_L^2)^{1/2} = 159$ mA.

9. What is the total current in the following circuit?

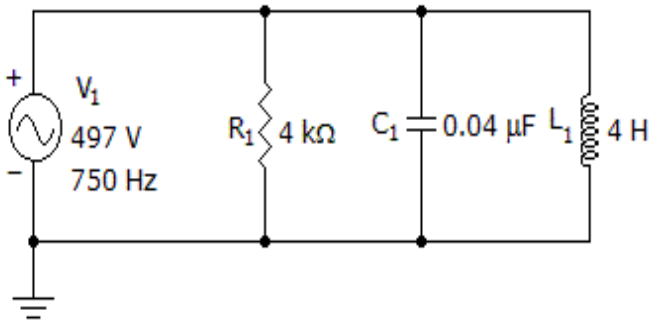


A) 56.6 mA **B) 141 mA** C) 91 mA D) 244 mA

Since they are in parallel, the voltage over R, C and L is the same: the source voltage 497 V. The current through R is I_R=Vs/R, through C is I_C=Vs/Xc, and through L is I_L=Vs/X_L, where Xc=1/(2πf·C) and X_L = 2πf·L. Thus Xc=5305Ω and X_L = 18850Ω. This gives a current of I_R= 12 mA, I_C = 9 mA and I_L=3 mA.
However, the current will lag the source voltage (-90° phase shift) in the inductor (voltage leads current in an inductor, therefore current lags voltage in an inductor), it will lead the voltage (+90° phase shift) in the capacitor, and will be in phase (0° phase shift) in the resistor. Thus, we must add the total current as vectors: $\boldsymbol{I_T = I_R + I_C + I_L}$ (see figure below), and its magnitude is $|\mathbf{I_T}| = \text{sqrt}(I_R^2 + (I_C - I_L)^2)$. This comes out to be 141 mA.



10. What is the phase angle between the current and the source voltage in the circuit of problem 9?



A) 61.4° **B) 28.5°** C) -28.5° D) -61.4°

Since the voltage is the same across all the components, we want to know the phase angle the current makes to the voltage (see figure in problem 9). From above, the phase angle is $\varphi = \tan^{-1}((I_C - I_L)/I_R)$, which is 28.5°. Hence net reactance of the circuit is capacitive, and the current will lead the voltage across the equivalent impedance of the circuit.

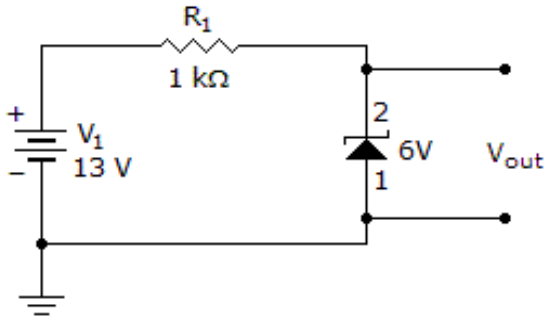
Multiple Choice Questions-2 (40% total).

There is only **one** correct answer so you must **choose the best answer**. Answer A, B, C, … (Capital letters). Correct answers give +4; incorrect or blank answers give 0.

Again, **on the answer sheet you turn in** use a table similar to the following:

Question	11	12	13	14	15	16	17	18	19	20
Answer	**B**	**F**	**C**	**A**	**D**	**B**	**A**	**+4**	**C**	**D**

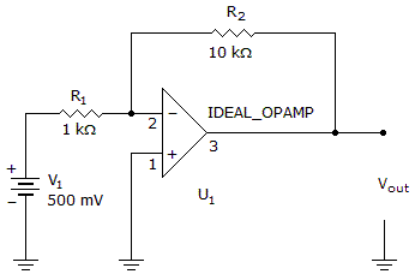
11. What is the current through the Zener diode?



A) 0 mA **B) 7 mA** C) 8.3 mA D) 13 mA

Since $V_1 > V_{out}$, the voltage across the Zener diode will be a constant 6 V. Thus, the voltage drop across the resistor, R_1, will be V_1-V_z. Since the current through the resistor will also pass through the Zener, the current is driven by the voltage drop across R_1: $I = (V_1 - Vz)/R = (13\text{-}6)V / 1\ k\Omega = 7$ mA is the current through the diode.

12. What is the output voltage of the following circuit?



A) 15 V D) -15 V
B) 50 mV E) -50 mV
C) 5V **F) -5 V**

The op-amp will stabilize its output when there is no potential difference across its inputs. We have here that $V_+ = 0$ V, so the potential at V_- must also = 0V. There is a potential difference across voltage divider of $R_i = R_1$ and $R_f = R_2$ of $V_{in} - V_{out}$ that drives a current
$I = (V_{in}\text{-}V_{out}) / (R_i + R_f)$. This current across R_1 will drop the input voltage V_i by an amount $I*R_1$, and thus the voltage at the inverting input, $V_- = V_i - I*R_1$. But this

voltage must be 0 when the amplifier is stabilized. Therefore, $0 = V_i - I*R_1 = V_i - [(V_{in}-V_{out}) /(R_1+R_2)]* R_1$. This allows us to solve for the gain $G = V_{out}/V_i = -R_2/R_1$, where negative sign is because the amplifier inverts the signal here. Hence, the system above has a gain of $-10k\Omega/1k\Omega= -10$, and $V_{out}=-10*V_{in}=-5V$.

13. If the input to a comparator is a sine wave, the output is a:

A) ramp voltage
B) sine wave
C) rectangular wave
D) sawtooth wave
E) All of the above

In a comparator there is no feedback. Thus, any difference in the inputs of the operational amplifier will result in the output swinging to full scale in a direction that is consistent with trying to bring its inverting input to the same voltage as its non-inverting input. Thus, if $V_+>V_-$, the output will swing positive in an attempt to raise V_-. Since there is no feedback, the output will swing to the positive supply voltage. The opposite is true for $V_->V_+$.

14. A Bi-Polar Juntion Transistor is a _____-controlled device. The JFET is a _____ -controlled device:

A) current, voltage
B) current, current
C) voltage, voltage
D) voltage, current

The base current controls the collector-emitter current in a BJT, whereas the voltage on the gate of a JFET controls the width of the source to drain conduction channel.

15. How will electrons flow through a p-channel JFET?

A) from source to drain
B) from source to gate
C) from drain to gate
D) from drain to source

The flow of major carriers in JFET is from SOURCE to DRAIN (as their name indicates). For an n-FET, the Source-Drain channel is n-type material and the major carriers are electrons that flow Source to Drain (the conventional +carrier current is from Drain to Source). For a p-FET, the Source-Drain channel is p-type material and the major carriers are holes (+current) that flow from Source to Drain, thus the conventional current is source to drain. However, the question asks which way the electrons will flow, and this is the opposite. That is, the -carrier current, electrons, flow from Drain to Source.

16. What is meant by 'pink noise'?

A) The noise has a frequency equal to that of pink light.
B) **Most of the noise power is concentrated at low frequencies**
C) Most of the noise power is concentrated at high frequencies.
D) The noise has a uniform spectrum.

Pink noise refers to the noise power at lower frequencies being higher than at high frequencies. This is usually manifested by longer terms drifts of the DC level.

17. The logic gate that will have HIGH or "1" at its output when any one of its inputs is HIGH is:

A) an OR gate
B) an AND gate
C) a NOR gate
D) a NOT gate

Note that any ONE of its inputs is high. That means input 1 OR input 2 will generate a HIGH at the output. If input 1 and input 2 are BOTH high, the output will be LOW.

18. Simplify the expression $Y = A\overline{B}D + A\overline{BD}$:

A) $Y = AB$
B) $Y = \overline{D}$
C) $Y = BCD$
D) $Y = A\overline{B}$
E) $Y = \overline{ABD}$

Printing mistake (I've been microsofted), it should have been:
$Y = A \cdot \overline{B} \cdot D + A \cdot \overline{B} \cdot \overline{D}$. In which case the expression would not depend on the value of D (it could be true or false) and answer D) above would have been correct. As it is, the expression reduces to $Y = A(\overline{B} + \overline{D})$ which is not given as an option. Therefore, you all get 4 free points (merry Christmas!).

19. What is the resolution of a 6-bit analogue (0-5V) to digital data converter?

A) 4% B) 64% **C) 1.56%** D) 15.6% E) 7.8%

Percentage resolution is the percentage of the full-scale output range that a change of 1 bit will give. Here, 6 bits will give 64 different output levels. So a change of 1 bit will give 5V / 64 = 0.078125 V change. As a percentage of the full-scale output, 5 V, this is: (5V/64)/5V*100 = 1/64 * 100 = 1.56 %

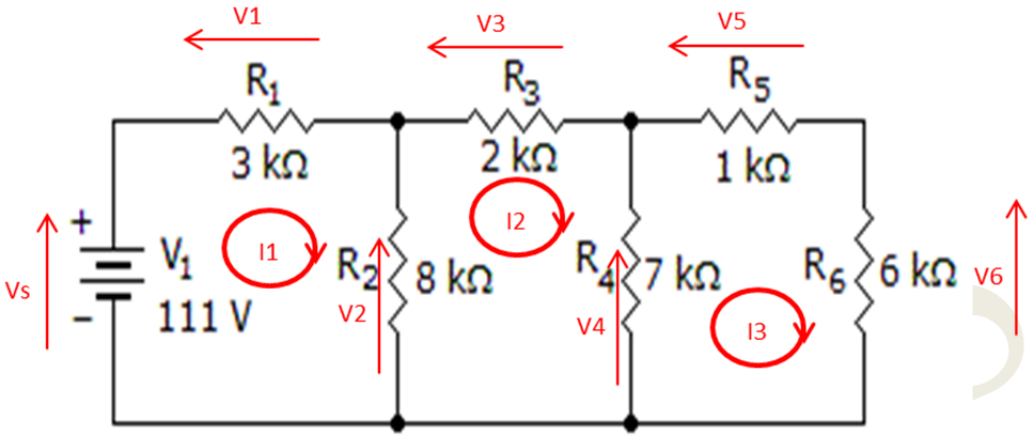
20. How many storage locations are available when a memory device has twelve address lines?

A) 144 B) 512 C) 2048 **D) 4096**

With 12 address lines, I can form a 12-bit binary number. With a 12 bit binary number, I can count from 0 to 4095, or access 4096 different locations (the address for the first location is 0).

Calculations (20% total)

21. What is the power dissipated by R_2, R_4, and R_6? (7%)



Mesh gives
$VS–V1–V2 = 0$
$V2–V3–V4 = 0$
$V4–V5–V6 = 0$

Using KVL on three loops, your equations will be:
$111V – R_1*I_1 – R_2*(I_1-I_2) = 0$
$R_2*(I_1-I_2) – R_3*I_2 – R_4*(I_2 – I_3) = 0$
$R_4*(I_2-I_3) – R_5*I_3 – R_6*I_3 = 0$

Expand to:
Equation 1: $111V – (R_1+R_2)*I_1 + R_2*I_2=0$
Equation 2: $R_2*I_1 – (R_2+R_3+R_4)*I_2 + R_4*I_3 = 0$
Equation 3: $R_4*I_2 – (R_4+R_5+R_6)*I_3 = 0$ ***Obtaining Equations +3***

Substituting in values:
Equation 1: $111V - 11k\Omega \cdot I_1 + 8k\Omega \cdot I_2 = 0.$
Equation 2: $8k\Omega \cdot I_1 - 17k\Omega \cdot I_2 + 7k\Omega \cdot I_3 = 0.$
Equation 3: $7k\Omega \cdot I_2 - 14k\Omega \cdot I_3 = 0.$

Solving the equations will give.
$I_1 = 17.73mA$, $I_2 = 10.5mA$, $I_3 = 5.25mA$. ***Solving for currents +1***

Go back to circuit you will find that,
$P_2 = (I_1–I_2)^2*R_2 = 417mW.$
$P_4 = (I_2–I_3)^2*R_4 = 193mW.$
$P_6 = I_3^2*R_6 = 166mW.$ ***Getting proper powers +3***

Another method to solve this is by using equivalent resistance:
Equivalent resistance of R_3 through R_6 is $R_{eq1} = R_3+R_4//(R_5+R_6)$
Total equivalent resistance of circuit $R_{eq} = R_1 + R_2//R_{eq1}$

This gives R_{eq1} = 11/2 kΩ = 5.5kΩ, R_{eq} = 169/27 kΩ = 169000/27 Ω = 6259Ω, and the total current is:
$I_T = V/R_{eq}$ = 111V /(169000/27 Ω) = 17.73 mA. ***Getting the proper total current +3***

Now, This It is split between R_2 and R_{eq1}, but the voltage at the top of R_2, V_2, is equal to the voltage at the top of R_{eq1} as is given by $R_2//R_{eq1} * I_T$ = 57.8V. (or V_s-I_T*R_1)) So, now we know that the power in R_2 is V^2/R_2 = **417.6 mW**.
To do this in terms of currents, since V=I*R, we have $I_2*R_2 = I_{eq1}*R_{eq1}$, and from Kirchoff's Current law we have that $I_T = I_2 + I_{eq1}$.

This gives $I_2 = I_T/(1 + R_2/R_{eq1})$ = 7.22 mA, and I_{eq1} = 10.5 mA (from $I_{eq1} = I_T - I_2$), and $P_2 = I_2^2*R_2$= **417.6 mW** ***Either method to get power in R_2 gives +1***

Now we can do the same thing for the part of the circuit with R_3 through R_6, where the current entering R_3 is I_{eq1} = 10.5 mA. This is identical to what we have just done

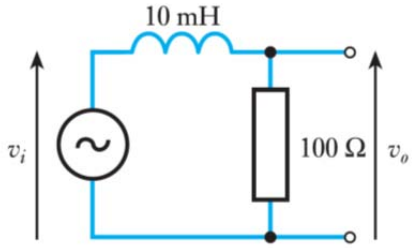
Now we have $R_{eq2} = R_5+R_6$, and R_4 is in parallel with R_{eq2}.
The current through R_3, I_{eq1}, so the voltage at the top of this parallel pair,
$V_4 = V_2 - I_{eq1}*R_3$ = 36.8 V, and the power in R_4 is V_4^2/R_4 = **193.3 mW**
Or again in terms of currents, I_{eq1} is split between R_{eq2} and R_4 such that
I_{eq1} = 10.5 mA = I_4+I_{eq2}, and $I_4 *R_4 = I_{eq2}*R_{eq2}$
We again have $I_4 = I_{eq1}/(1+R_4/R_{eq2}) = 10.5\text{ mA}/(1 + R_4/(R_5+R_6))$

Now, happily for us, Req_2 = 7kΩ, the same as R_4, so the current is split equally and gives
$I_4 = Ieq_2$ = 5.25 mA

This last current flows through both R_5 and R_6 since they are in series. So, the power through the resistors R_2, R_4 and R_6 is

$I_2^2*R_2$ = **417.6 mW**
$I_4^2*R_4$ = **193.3 mW**, and
$I_{eq2}^2*R_6$ = **165.6 mW** ***Obtaining power in R_4 and R_6 +3***

22. For the circuit below, with $v_{in}(t) = V_{in}\cdot\cos(\omega\cdot t)$ Volts, find the transfer function $H(\omega) = V_{out}/V_{in}$, and sketch the response versus frequency. (4%)

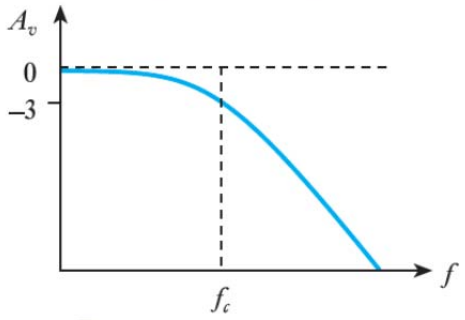


Using complex notation, the output voltage across the impedance divider is $Vo = Vi*Z_R/(Z_R+Z_L)$. Using complex notation, the response function is:

$$\frac{v_o}{v_i} = \frac{\mathbf{Z}_R}{\mathbf{Z}_R + \mathbf{Z}_L} = \frac{R}{R + j\omega L} = \frac{1}{1 + j\omega\frac{L}{R}} = \frac{1}{1 + j\frac{\omega}{\omega_c}} = \frac{1}{1 + j\frac{f}{f_c}}$$

+2 points

Where the cutoff frequency is given by $T=L/R = 10^{-4}$ s, so that $\omega_c=1/T=10^4$ rad/s. The frequency is then $f_c = \omega_c/(2\pi) = R/(2\pi L) = 1.59$ kHz. Thus the response function would look like:



+2 points

With fc = 1.59 kHz.

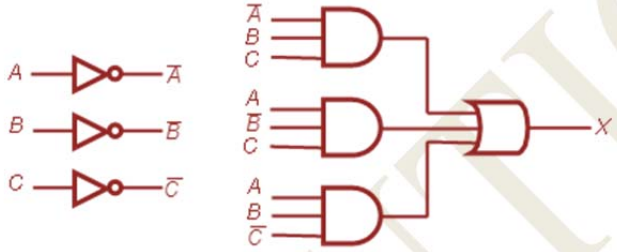
23. Write a truth table, Boolean expression and design a logic circuit to take three inputs, A, B and C, and produce a single output X, such that X is true if, and only if, precisely two of its inputs are true. (9%)

Truth table (***+3 points***)

A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

By inspection, the Boolean expression is $X = \bar{A}BC + A\bar{B}C + AB\bar{C}$ (***+3 points***)

Which can be implemented as:



(***+3 points***)

Note that this cannot be simplified. If one looks at a Karnaugh map, one sees there are no legal combinations (horizontal lines of columns or vertical lines of rows) of 1's that can be combined.

	AB			
C	00	01	11	10
0	0	0	1	0
1	0	1	0	1