The Norwegian University of Science and Technology ENGLISH

Department of Physics

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EXAM IN TFY 4185 Measurement Technique/Måleteknikk

1 Dec 2014 Time: 09:00-13:00

Number of pages: 14

Permitted aids:

- 1) Dictionary (ordinary or bi-lingual)
 - 2) All calculators
 - 3) 1 side of an A5 sheet with printed or handwritten formulas permitted

You can answer in either Norwegian or English. The weight for each multiple-choice question is 4%, the weight for each calculation problem is given in parenthesizes.

The solutions to the multiple choice-questions are given in a light red colour. I have given the justification for the solution in the dark red colour for information, but will only grade the multiplechoice answer.

Multiple Choice Questions-1 (40% total).

There is only **one** correct answer so you must **choose the best answer**. Answer A, B, C... (Capital letters), or leave the answer blank. Correct answer gives +4; incorrect answers give 0, and blank (unanswered) gives +1.

Write the answers for the multiple choice questions **on the answer sheet you turn in** using a table similar to the following:

Question	1	2	3	4	5	6	7	8	9	10
Answer	A or C	С	A	С	D	С	D	B	B	A

1. Calculate the magnitude of the current I in the following circuit:



Kirchoff's Current Law \Rightarrow 3A - 10A - I = 0. \therefore I = -7A, or I is actually flowing into the junction. This is from Storey's book, and I notice he is more cavalier with "magnitude" than a physics major would be. Hence I must also accept answer C

2. Calculate the output voltage V of the following circuit:



A Voltage Divider: The same current, I, flows through the 2 resistors. $\therefore I = (10V-4V)/R_{tot}$. Since the same current is flowing through all the resistors, they are in series and $R_{tot} = \Sigma R_i = 30\Omega + 60\Omega = 90\Omega$. Although it is not necessary to calculate this current, it will be: $I = 6 V/90\Omega = 0.067 A$.

The voltage drop across resistor 1 is $10V \cdot V = I \cdot R_1$, and the voltage drop across resistor 2 is $V - 4V = I \cdot R_2$. It does not matter which one we choose to calculate V. That is, both gives: $(1) V = 10V \cdot (10V \cdot 4V)/R_{tot} \cdot R_1 = 6V$ (2) $V = (10V \cdot 4V)/R_{tot} \cdot R_2 + 4V = 6V$

3. If a sinusoidal voltage $v = V_p \sin \omega t$ is applied across a capacitor, *C*, what is the average value of the power dissipated in the capacitor?

A) 0

B) CV_p^2 C) V_p^2/C D) $2CV_p^2$

While there will be energy within the capacitor, it stores energy for one part of the cycle and returns it to the circuit during the other part of the cycle. Thus, the average power dissipated in the capacitor (or inductor) is zero

4. A moving-coil meter produces a full-scale deflection for a current of 100 μ A and has a resistance of 500 Ω . Select a series resistor (R_{SE}) that will turn this device into a voltmeter with an full scale deflection of 1 V.



The full scale deflection current, $I_{fsd} = 100 \mu A = 1 \times 10^{-4} A$ with a meter resistance $R_m = 500 \Omega$. This FSD occurs when the voltage across the meter is: $V_{fsd} = I_{fsd} \cdot R_m = 0.05 V$. Now we will measure a signal of V = 1V with series resistance R_{SE} so that we still get the same V_{fsd} across the meter. This is yet another voltage divider where we specify the voltage drop across R_m as $V_{fsd} = 0.05V$ and are asked to specify R_{SE} for a given input voltage, V = 1V.

The current through the two resistors is the same and $I = V/(R_{SE} + R_m)$. The voltage drop across the series resistor should be: $(V-V_{fsd}) = I \cdot R_{SE}$, and the voltage drop across the meter will be $(V_{fsd}-0V) = I \cdot R_m$. The latter saves a subtraction and we have that $V_{fsd} = [V/(R_{SE} + R_m)] \cdot R_m$. You can either substitute in V = IV, $V_{fsd} = 0.05V$ and

 $V_{fsd} = [V/(R_{SE} + R_m)] \cdot R_m$. Tou can either substitute in V = IV, $V_{fsd} = 0.05V$ and $R_m = 500\Omega$, and do simple arithmetic to get $R_{SE} = 9.5 k\Omega$, or do simple algebra on the equation to recover the book formula $R_{SE} = V \cdot R_m / V_{fsd} - R_m = V / I_{fsd} - R_m$, and substitute in there.

5. Use the principle of superposition to determine the output voltage V of the following circuit.



To do superposition, we replace all voltage sources (except the one for which you are calculating) by wires, and replace all current sources (except the one for which you are calculating) by open circuits. Here, let us first short out the 30V power supply with a wire. Then going from the 15V power supply we have R_1 in series with the parallel pair of R_2 and R_3 . Or R_1 in series with R_{23} , where $R_{23} = (1/R_2 + 1/R_3)^{-1}$. The total resistance is therefore $R_{tot} = R_1 + R_{23} = R_1 + R_2 \cdot R_3 / (R_2 + R_3)$, and a handy shortcut is that for two resistors of the same value in parallel, the effective parallel resistance is half the resistance. Thus, $R_{tot} = 100\Omega + \frac{1}{2} \cdot 100\Omega = 150\Omega$. The total current is therefore $I = 15V/150\Omega = 0.1A$.

This current is split between R_2 and R_3 , but in this special case, where they have the same value of resistance, the current is split equally between the R_2 and R_3 branches. Hence, the current through R_3 , $I_3 = \frac{1}{2} \cdot 0.1A = 0.05A$, and the voltage across R_3 is: $V_3 = I_3 \cdot R_3 = 0.05A \cdot 100\Omega = 5V$.

Now we put the 30V power supply back in the circuit, and calculate the voltage across R_3 when we short out the 15V power supply. Now we see we go from the 30V power supply across R_2 in series with the parallel pair R_1 and R_3 . Again, since $R_1 = R_2 = R_3 = 100\Omega$, this is going to be the same total resistance as we did before ($R_{tot} = 150\Omega$), the current will be twice as much (since the power supply has twice the voltage), so $I_{tot} = 0.2A$, and this will be split equally across the R_1 and R_3 branches, giving $I_3 = 0.1A$. Therefore, this power supply puts a voltage across R_3 of: $V_3 = I_3 \cdot R_3 = 0.1A \cdot 100\Omega = 10V$. The total voltage across R_3 is therefore the 5V from the 15V power supply, plus the 10V from the 30V power supply, or 15V.

The shortcut here is that 2 resistors of equal value in parallel gives you a net resistance of half the resistor value, and the current will split equally between the two resistor paths. The next realization is that shorting out either the 15V supply or the 30V supply gives the same resistor network with the same values, but 2x the voltage will give 2x the current, and thus 2x the voltage drop across R_3 .

6. Which one of the following statements is correct in relation to alternating waveforms:

- A) In a capacitor, the voltage leads the current.
- B) In an inductor, the voltage lags the current.
- C) In a capacitor, the current leads the voltage.
- D) In an inductor, the current leads the voltage.

One can remember either the mnemonic ELI the ICE man, or CIVIL. Basically, E(V) leads I in and inductor (L), and I leads E(V) in a capacitor (C). Thus choice c) is correct.

7. Which of the following combination of components represents an impedance of $110 + j 314 \Omega$ at a frequency of 100 Hz?

- A) A resistor of 100 Ω in series with a capacitor of 5 μ H
- B) An inductor of 50 mH in series with a capacitor of 5 μ H
- C) A resistor of 314 Ω in series with an inductor of 5 mH
- D) A resistor of 110 Ω in series with an inductor of 500 mH

First, the angular frequency is $\omega = 2 \cdot \pi f = 628$ rad/s. A resistor has purely real impedance while capacitors and inductors have purely imaginary impedances. Thus the real part has to be a resistor of 110 Ω . Our choice is a capacitor, which would have a negative, complex impedance (I leading V by 90°) so the only way to get a positive imaginary result is to have an inductor. The impedance of an inductor is $Z_L = j(\omega \cdot L)$ which must equal 314 Ω at this frequency. Thus, the inductor is 314 Ω /628 rad/s = 0.500 H, or 500 mH in series with 110 Ω resistor. And, of course, the capacitors in answers A and B should be μ F, not μ H.

8. The switch in the following circuit closes at t = 0. If the capacitor is initially discharged, calculate the time, t, at which the voltage on the capacitor is 12.6V.



Initially when the switch is closed, there is no charge on the capacitor so that the voltage across the capacitor is 0 (one could also look at it from the point of view that the instantaneous change in current brought about by closing the switch is a current changing infinitely fast, and therefore represents an infinite frequency. The impedance of a capacitor to an infinite frequency,-j/(ω ·C), is zero. No impedance=no voltage drop!). As the current flows, the charge on the capacitor grows, and hence the voltage slowly grows and eventually reaches 15V. The equation for the change in voltage is: $v = V_f + (V_i - V_f) \cdot e^{-t/\tau}$. Solving this equation for time gives us: $t = -\tau \cdot \ln[(v - V_f)/(V_i - V_f)]$, where $V_i = 0$, $V_f = 12.6 V$, and $\tau = R \cdot C = 50 \times 10^3 \Omega \cdot 33 \times 10^{-6} F = 1.65 \sec(/rad)$. Substituting in give the time to charge the capacitor to 12.6 V is 3 s.

9. When unconnected to any other circuit elements, an amplifier has a voltage gain of 20, an input resistance of 500 ohms and an output resistance of 50 ohms. The amplifier is connected to a voltage source that produces an output voltage of 1 V and has an output resistance of 75 ohms (when unconnected to any other circuit elements), and to a load resistance of 800 ohms. What will the voltage across the load resistor be when this circuit is connected?

A) 20 V B) 16.4 V C) 18.8 V D) 17.4 V

Now both the input voltage source and the output of the amplifier can be loaded down. For example, when unconnected, the voltage source produces an output voltage of 1 V with an internal output resistance of 75 Ω . However, this impedance, R_o will be in series with any load resistance, R_L , that I place on the voltage source. Thus, R_o and R_L form a voltage divider so that the voltage that will actually appear across the load will be $V_{s'}(R_{s}+R_{L})$ times R_L . In this case, the load is actually the input resistance of the amplifier, R_i , stated to be 500 Ω . Now, if this resistance were very much greater than the source output resistance, we could ignore the source output resistance and the voltage across the amplifier would be 1V. But here they are relatively similar, and the voltage across the input of the amplifier will be: $V_{s'}(R_s+R_i) \cdot R_i=1V/(575\Omega) \cdot 500\Omega = 0.870$ V.

Similarly, the amplifier will create a voltage $A_v \cdot V_i$, and drive this across an output impedance of 50 Ω . However, this output impedance is in series with the load resistor of 800 Ω . This means that the voltage that appears across this load is actually part of a voltage divider formed by R_o and R_L . So the voltage that appears across the load will be $A_v \cdot V_i/(R_o + R_L)$ times R_L . Now if R_L is very large compared to R_o , we can neglect R_o . Unfortunately here they are not so very different. The actual voltage across the load, the true output voltage of the amplifier, will be the divided voltage given above. This is: $A_v \cdot V_i/(R_o + R_L) \cdot R_L = 20 \cdot 0.87V/(850\Omega) \cdot 800\Omega = 16.4 V$

10. What is the voltage gain of the amplifier in question 9 when it is connected to the source and load resistance?

A) 18.9 B) 20 C) 17.4 D) 16.4

Since the input voltage, calculated in the previous problem, is 0.87V, and the output voltage is 16.4V, the effective gain of the amplifier is given by $V_{\varrho}/V_i = 16.4/0.87 = 18.8$

Multiple Choice Questions-2 (40% total).

There is only **one** correct answer so you must **choose the best answer**. Answer A, B, C, ... (Capital letters), or leave the answer blank. Correct answer gives +4; incorrect answers give 0, and blank (unanswered) gives +1.

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Question	11	12	13	14	15	16	17	18	19	20
Answer	D	B	B	D	С	A	С	B	В	D

11. What is the voltage gain of this circuit?



Here the feedback is derived from the output voltage that is divided across the resistor network formed by R_1 and R_2 . Since no current flows into the amplifier (for an ideal amplifier), the feedback voltage appearing at the inverting input, V., is given by $V_f = V_o \cdot R_2 / (R_1 + R_2)$. When the feedback voltage is equal to the input voltage, $V_i = V_f$, there will be no voltage difference across the inputs of the amplifier and the output voltage will stabilize. The gain, is the ratio of the output to input voltage, so, substituting Vi into the feedback voltage equation allows us to calculate the gain as: $V_0/V_i = (R_1+R_2)/R_2$. Substituting in 10 k Ω and 1 k Ω for R_1 and R_2 , gives a gain of 11.

12. A Zener diode:

- A) Has a high forward voltage rating
- B) Has a sharp breakdown at low reverse voltage
- C) Is useful as an amplifier
- D) None of the above

A Zener diode is a "normal" diode with the same forward voltage rating. However, the "doping" of the material is set such that it will undergo Zener and/or avalanche breakdown at a particular voltage that is much lower than the typical breakdown voltage of a "normal" diode.

13. A long section of p-type semiconductor material:

- A) Is positively charged
- B) Is electrically neutral
- C) Has an electric field directed along its length
- D) None of the above

A p-type semiconductor is created by adding a "dopant" to the intrinsic semiconductor. For Si, the dopant is usually boron (B) that will contribute 3 rather than 4 valence electrons to the bonding. This leaves an extra "hole" in the material. However, the total number of positive and negative charges in the material is the same, and so the material is electrically neutral. Only when it is in contact with an n-type material will the holes drift across the junction region and recombine, leaving the B atoms with one fewer positive charge, and therefore negatively ionized. This drift across the junction will then create an electric field. However, with no junction, there is no charge or no electric field on the material and it is neutral.

14. The drain current in JFET is always controlled by:

- A) Voltage drop along the channel
- B) Magnitude of the depletion
- C) Channel length
- D) Reverse-bias at the gate

The JFET will have a channel of one type of doped semiconductor (usually n) and a gate of the oppositely doped semiconductor. When the gate is reversed biased relative to the channel, the depletion region will expand and increase the resistance of the channel. This will then control the current from the drain to the source. While the voltage drop along the channel will change the current in the ohmic region, and the size of the depletion region changes the resistance of the channel, it is the reverse bias of the gate that determines and controls these two, and hence the drain current. So the best answer is D.

15. A bipolar junction transistor is in the saturation region if:

- A) Base-emitter junction is reverse-biased and base-collector junction is forwardbiased.
- B) Both the junctions are reverse-biased.
- C) Both the junctions are forward-biased.
- D) Base-emitter junction is forward-biased and base-collector junction is reversebiased.

At low values of V_{CE} the transistor is in the saturation region. At these low values of V_{CE} , the transistor action does not occur and the transistor is in an "on" condition. This means that, assuming the base potential creates a forward bias between the base and emitter, there will also be a forward bias between the base and the collector due to the small potential between the collector and emitter, V_{CE} . Under forward bias the depletion regions are physically very small, and a potential between the collector and the emitter drives the collector majority charge carriers into the base, where they recombine. However, it also drives the base majority charge into the emitter. This current will increase with V_{CE} until we reach a point where the collector becomes forward biased relative to the base, and transistor action can occur. Since both junctions are conducting and on, this is called saturation.

C = 64 nF v_i $R_1 = R_C = 2.7 \text{ k\Omega}$ $R_2 = R_E = 10 \text{ k\Omega}$ $R_E = 1 \text{ k\Omega}$

0 V

16. In the following circuit, how is the input to the base filtered?

- A) It is high-pass filtered.
- B) It is low-pass filtered.
- C) It is band-pass filtered.
- D) It is notch-filtered

Since the input, v_i , must go across the capacitor to reach the base, only the high frequency components will be able to get across. This is because the impedance of the capacitor, $1/(j\omega C)$, is very low at high frequencies so that it appears as a wire. At low frequencies, it appears as very high impedance, approaching an open circuit condition that blocks low frequencies from the base. Thus, the input to the base is <u>high-pass filtered</u>.

17. Determine the lower-frequency cut-off of the input to the base in the circuit of question 16.

A) 18 Hz B) 178 Hz C) 324 Hz D) 2037 Hz Because we are dealing with an AC signals, there will be capacitive coupling between V_{CC} and ground within the capacitor. Thus, the signal v_i will see the resistor to V_{CC} , R_1 , and the resistor to ground, R_2 , tied together as a parallel pair. This is what will be seen in the equivalent circuit of the transistor that we must use to determine AC voltages and currents. The input signal, v_i will therefore see a capacitor of 64 nF in series with the equivalent resistance, $R = R_1/R_2 = R_1 \cdot R_2/(R_1+R_2) = 33k\Omega \cdot 10 k\Omega/(33 k\Omega + 10 k\Omega) = 7.7$ $k\Omega$. The cut off frequency of this high-pass filter (we are taking the voltage across R) will be: $\omega_c = 1/(R \cdot C) = 1/(7.7x10^3 \Omega \cdot 64x10^{-9} F) = 2.04x10^3 rad/s$, and $f_c = \omega_c/(2\pi) = 324 Hz$.

18. What is the function of the following circuit?



- A) A modulo-12 counter.
- B) A modulo-10 counter.
- C) A modulo-8 counter.
- D) A modulo-6 counter.

Since both J and K are held high on each device, the clock will toggle the output of the J-K flip-flops on its negative going edge (the little circle on the clock input indicates this). However, since the clock of the second flip-flop is derived from the output of the first, it will switch half as often, and this will be repeated for the subsequent flip-flops. Thus, this configuration will form a ripple counter where the binary word $Q_3 Q_2 Q_1 Q_0$, will be the number of initial clock pulses received by the first, Q_0 , flip-flop. However, Q_1 and Q_3 are "anded" together in the NAND gate to form a negative going reset signal. So, the first time Q_3 and Q_1 are high we will reset the counter and start counting up from 0 again. One can see that counting up from 0 one will have Q_3 and Q_1 high for the first time when the binary count is 1010, or $1 \cdot 2^3 + 0 \cdot 2^2 + 1 \cdot 2^1 + 0 \cdot 2^0 = 10$. So the counter will count up to 10 and then reset itself back to 0, forming a modulo-10 or decade counter.

19. What is the resolution of a 10-bit analogue to digital data converter?

A) 0.00098% B) 0.098% C) 0.024% D) 0.41% A 10-bit ADC converter will break an analogue voltage range into 2^{10} separate levels, or a DAC will produce 2^{10} separate levels of analogue output. Thus, each step would be $V_{range}/2^{10} = V_{range}/1024$ volts large, which is the resolution of the device. If we divide by V_{range} and multiply by 100, we would get the resolution as a percentage. Thus, the resolution of a 10-bit converter is (1/1024) $\cdot 100\% = (0.00098) \cdot 100\% = 0.098\%$.

20. A signal contains components with frequencies up to 10 kHz, although no useful information is contained at frequencies above 6 kHz. What is the minimum frequency at which the signal should be sampled?

A) 6 kHz. B) 12 kHz. C) 14.4 kHz. D) 20 kHz. In order to prevent aliasing of frequencies, I would have to sample at twice the largest frequency in my signal, not the largest frequency in which I am interested. Those unwanted frequencies will still be there, and sampling at a lower rate would alias them into the band of frequencies in which I am interested.

Calculations (20% total)

21. You build the following circuit with $V_1 = 6 V$, and $R_1 = 30 \Omega$, $R_2 = 2 k\Omega$, $R_3 = 3 k\Omega$, $R_4 = 2 k\Omega$ and $R_5 = 1 k\Omega$.



a) Find the Thévenin Equivalent voltage, V_{th}=V_{OC}, of this circuit between point A and point B (2%)

Since no current flows through R_5 when the circuit between A and B is open, $V_{th} = Voltage \ across \ R_4 = V_1 \cdot R_4 / (R_1 + R_2 + R_3 + R_4) = \underline{1.707V}$

b) Find the Thévenin Equivalent Resistance, R_{th}, of this circuit between points A and B. (2%)

Replacing the voltage source, V_1 , with a short circuit, we can calculate the resistance between A and B. This puts R_4 in parallel with the series resistance formed by R_1 , R_2 and R_3 , and R_5 is in series with that parallel pair:

 $R_{th} = R_5 + (R_1 + R_2 + R_3)/R_4$ $R_{123} = R_1 + R_2 + R_3 = 5030 \ \Omega$ $R_{123}/R_4 = (5030)(2000)/(5030 + 2000) = 1431 \ \Omega$ $R_{th} = 1000 + 1431 = \underline{2431 \ \Omega}$

c) Find the Norton Equivalent Current, I_{SC}, of this circuit between points A and B. (1%)

If one has calculated the Thévenin voltage and resistance above, then then current is merely $I_{SC} = V_{th}/R_{th} = 1.707 \text{ V}/2431 \Omega = 702 \mu \text{A}.$

One could also calculate the current directly by shorting the circuit between A and B and then evaluate the current flowing there. Once A and B are shorted, the resistors R_4 and R_5 are in parallel, and this parallel network in in series with the series network formed by R_1 , R_2 and R_3 . The equivalent resistance for this network, connected to V_1 , is 5697 Ω , and the total current flowing is: $I_T = 6 \text{ V}/5697 \ \Omega = 1.05 \text{ mA}$. However, this is split between the two branches of the parallel network formed by R_4 and R_5 . The voltage at the top of this parallel pair is: $V' = V_1 \cdot (R_4//R_5)/(R1+R2+R3+(R_4//R_5)) = 0.702 \text{ V}$, and the current flowing through R_5 (and the shorted junction between A and B) is from Kirchoff's current law: $I_5 = I_T - I_4$, or using Ohms law to substitute for I_4 : $I_5 = I_T - V'/R_4$. Substituting in, we get that $I_{SC} = I_5 = 1.05 \text{ mA} - 0.702 \text{ V}/2000 \ \Omega = 702 \ \mu\text{A}$.

d) Redraw the Thévenin and Norton equivalent circuits. (2%)



e) A 2 k Ω load is connected between A and B. What is the voltage and current through this load? (2%)

 V_{th} is now divided between the two resistors, and the output voltage at A is: $V_{out} = V_{th} \cdot R_{load} / (R_{th} + R_{load}) = 1.707 \cdot 2000 / (2431 + 2000) = 0.770 \text{ V}$

The current is just $V_{th}/(R_{th}+R_{load}) = 1.707 \text{ V} / (2431 + 2000) \Omega = 385 \mu \text{A}$

f) Instead of connecting directly to the load, A and B are connected to a 741 operational amplifier in the circuit shown below, where R_6 is the 2 k Ω load. Estimate the voltage and current through the load, R_6 , now? (1%)



Now the operational amplifier presents a nearly infinite input resistance. We can see that the amplifier is run at a non-inverting gain of 1, or as a buffer amplifier. Thus, since the op-amp to first approximation does not draw any current, the voltage at the output is equal to the voltage at A, which is **1.707V**.

The current through the load is $I_{load} = V_{out}/R_{load} = 1.707 \text{ V}/2000 \Omega = 854 \mu\text{A}$

22. Digital logic

a) Show that circuits A and B are equivalent by setting up a truth table for the two circuits. What is the Boolean expression for the circuits? (2%)





Circuit A



The truth table for each circuit is:

Α	B	C1/C2
0	0	1
0	1	1
1	0	1
1	1	0

If we take C1=C2, and express it as a Boolean expression, we have De Morgan's law: $\overline{A} + \overline{B} = \overline{A \cdot B}$

b) For the following truth table, write down and simplify the Boolean expression. (2%)

```
A
   B
      C \mid X
        0
            0
0
    0
0
    0
       1
            1
0
        0
   1
            0
0
        1
            0
    1
    0
        0
            0
1
1
    0
        1
            1
        0
            1
1
    1
            0
        1
```

- $X = \overline{A} \overline{B} \overline{C} + A \overline{B} \overline{C} + A \overline{B} \overline{C}$ $= \overline{B} \overline{C} (A + \overline{A}) + A \overline{B} \overline{C}$
- $= \overline{B}C + AB\overline{C}$
- c) Using logic gates, implement the simplified Boolean expression of part b. (3%)

The circuit of the un-simplified expression, which will give 1 point, is:



The circuit for the simplified expression, which will give 3 points, is:



d) Re-draw the waveforms for the circuits below and include the waveform at the Q output. (3%)

