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Examination paper for TFY4185 Measurement Technique/ Måleteknikk

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Examination date: 11 August 2016

Examination time (from-to): 09:00 – 13:00

Permitted examination support material:

Single or Bi-lingual dictionary permitted
All calculators permitted
1 side of an A5 sheet with printed or handwritten formulas permitted

Other information:

Language: English

Number of pages:

Number of pages enclosed:

Checked by:

Date Signature

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ENGLISH

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EXAM IN TFY 4185 Measurement Technique/Måleteknikk

August 2016
Time: 09:00-13:00

Number of pages: 14

Permitted aids:
1) Dictionary (ordinary or bi-lingual)
2) All calculators
3) 1 side of an A5 sheet with printed or handwritten formulas permitted

Last page contains a listing of parameters for BJT transistors

You can answer in either Norwegian or English. The weight for each multiple-choice question is 4%, the weight for each calculation problem is given in parenthesizes.

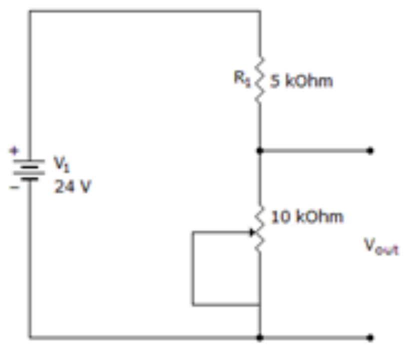
Multiple Choice Questions-1 (40% total).

There is only **one** correct answer so you must **CHOOSE THE BEST ANSWER**. Answer A, B, C… (Capital letters). Correct answers give +4; **incorrect or blank answers give 0**.

Write the answers for the multiple choice questions **on the answer sheet you turn in** using a table similar to the following:

Question	1	2	3	4	5	6	7	8	9	10
Answer	**D**	**A**	**C**	**D**	**B**	**A**	**B**	**A**	**B**	**C**

1. Calculate the voltage at point B in the following circuit:



A) 0 V, 4 V B) 0 V, 8 V C) 0 V, 12 V D) 0 V, 16 V

Maximum voltage drop occurs when the potentiometer is set at 10 kΩ. At this point, I = 24 V/15 kΩ, and the voltage drop across the potentiometer is $V_{out}=I*R$ = 24 V/15 kΩ * 10 kΩ = 16 V

2. When parallel resistors are of three different values, which has the greatest power loss?

A) The smallest resistance

B) The largest resistance

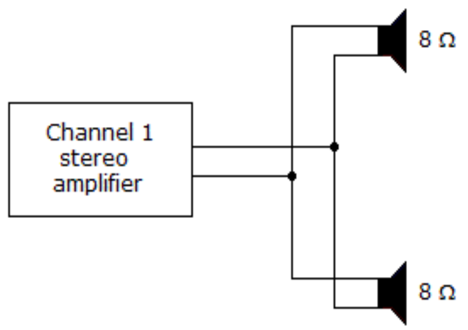
C) They all have the same poser loss

D) It depends on the values of the resistances

E) Not enough information given

Since the voltage drop is the same across all of the resistors, the one with the least resistance will have the most current (I = V/R). Hence, $P=I^2\cdot R= V^2/R$, and the smallest R has the greatest power loss.

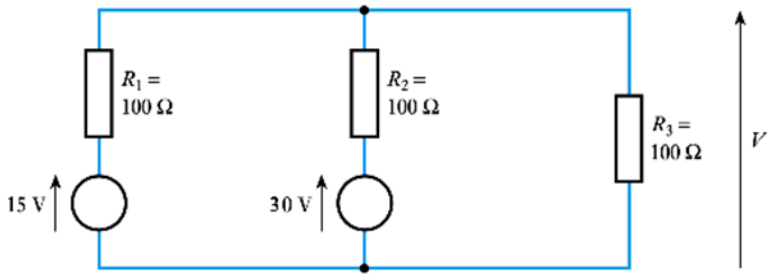
3. In the following circuit, Channel 1 of the stereo amplifier outputs 12 V to the speakers. How much total power is the amplifier delivering to the speakers?



A) 55 W B) 25 W <u>C) 35 W</u> D) Not enough information given

The two speakers are in parallel presenting a net load of R_L=(8Ω·8Ω)/(8Ω+8Ω) =4Ω. The 12 V across this load will produce a current I = 12 V/ 4Ω = 3A. The power will be this current times the voltage (12V * 3 A = 36 W). It will also be this current squared times the net resistance (9 A^2 * 4 Ω = 36W).

4. Determine the output voltage V of the following circuit:



A) 5 V B) 7.5 V C) 12 V <u>D) 15 V</u>

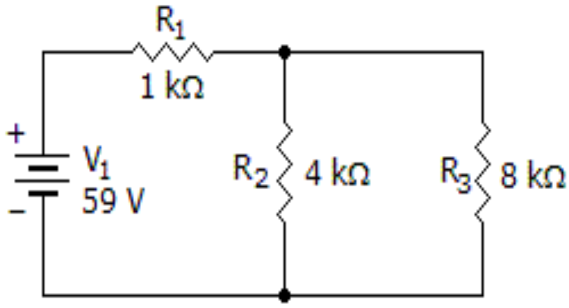
This problem cries out for superposition. To do superposition, we replace all voltage sources (except the one for which you are calculating) by wires, and replace all current sources (except the one for which you are calculating) by open circuits. You can do this problem in your head by noting that 2 resistors of equal value in parallel gives you a net resistance of half the resistor value, and the current will split equally between the two resistor paths. The next realization is that shorting out either the 15V supply or the 30V supply gives the same resistor network with the same values, but 2x the voltage will give 2x the current, and thus 2x the voltage drop across R_3.

To grind through the superposition, let us first short out the 30V power supply with a wire. Then going from the 15V power supply we have R_1 in series with the parallel pair of R_2 and R_3. Or R_1 in series with R_{23}, where $R_{23} = (1/R_2 + 1/R_3)^{-1}$. The total resistance is therefore $R_{tot} = R_1 + R_{23} = R_1 + R_2 \cdot R_3/(R_2+R_3)$, and the mental arithmetic is that for two resistors of the same value in parallel, the effective parallel resistance is half the resistance. Thus, $R_{tot} = 100\Omega + ½ \cdot 100\Omega = 150\Omega$. The total current is therefore $I = 15V/150\Omega = 0.1A$.

This current is split between R_2 and R_3, but in this special case, where they have the same value of resistance, the current is split equally between the R_2 and R_3 branches. Hence, the current through R_3, $I_3 = \frac{1}{2} \cdot 0.1A = 0.05A$, and the voltage across R_3 is:
$V_3 = I_3 \cdot R_3 = 0.05A \cdot 100\Omega = 5V$.

Now we put the 30V power supply back in the circuit, and calculate the voltage across R_3 when we short out the 15V power supply. Now we see we go from the 30V power supply across R_2 in series with the parallel pair R_1 and R_3. Again, since $R_1 = R_2 = R_3 = 100\Omega$, this is going to be the same total resistance as we did before ($R_{tot} = 150\Omega$), the current will be twice as much (since the power supply has twice the voltage), so $I_{tot} = 0.2A$, and this will be split equally across the R_1 and R_3 branches, giving $I_3 = 0.1A$. Therefore, this power supply puts a voltage across R_3 of: $V_3 = I_3 \cdot R_3 = 0.1A \cdot 100\Omega = 10V$. The total voltage across R_3 is therefore the 5V from the 15V power supply, plus the 10V from the 30V power supply, or 15V.

5. What is the power dissipated by R1, R2, and R3?



A) P1 = 0.1 W, P2 = 0.3 W, P3 = 0.1 W
B) P1 = 0.3 W, P2 = 0.5 W, P3 = 0.2 W
C) P1 = 0.5 W, P2 = 0.9 W, P3 = 0.5 W
D) P1 = 1.0 W, P2 = 1.8 W, P3 = 0.9 W

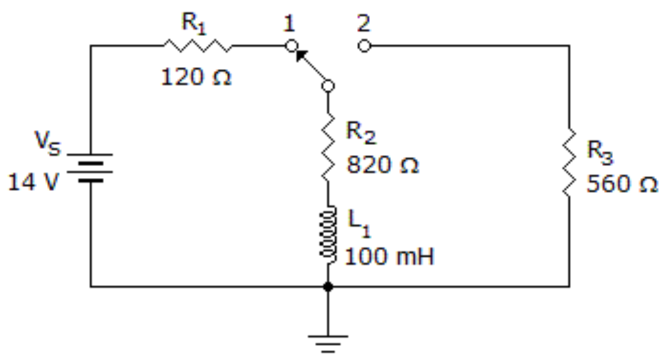
The total current is flowing across R_1 in series with the parallel pair R_2 and R_3 that have an equivalent resistance $R_{//} = (R_2 \cdot R_3)/(R_2+R_3)$. So the total resistance is R_T given by 1 kΩ + (4 kΩ ·8 kΩ) / (4 kΩ + 8 kΩ), or R_T = 3.67 kΩ. The total current is $I = V_1/R_T$, or I = 59V/3.67 kΩ = 16.1 mA. This current flows through R_1 causing the supply voltage to drop $I \cdot R_1$ volts to V_2= 59V - 0.0161A·1000 Ω = 42.9 V. This voltage across will create a current I_2=42.9 V/R_2, and a current I_3=42.9V/R_3 across R_3. Substituting in values, we have I_1= 16.1 mA, I_2= 10.7 mA and I_3 = 5.3 mA. Therefore the power dissipated in the three resistors = $I^2R \Rightarrow P1 = (16.1\text{ mA})^2 \cdot 1$ kΩ = 0.26W, $P2=(I_2^2 \cdot R_2) = V_2^2/R_2$ = 0.46 W, and $P3=(I_3^2 \cdot R_3) = V_2^2/R_3$ = 0.23 W.

6. With a 500 kHz signal source, what would be the value of a capacitor yielding a capacitive reactance of 1 kΩ?

A) 320 pF B) 3.8 nF C) 318 nF D) 2 μF E) 2 F

$X_C = 1/(\omega*C)$ is given as 1 kΩ, and $\omega = 2*\pi*f$, where f is 500 kHz. So, solving for C and substituting in we get $C = 3.18\text{x}10^{-10}$ F, or 318 pf. The best answer is 320 pF

7. In the following circuit that has stabilized, what will the voltage be across R_3 at a time t = 25 ms after the switch is moved to position 2?



A) 4 V **B) 5.9 V** C) 8.6 V D) 9.9 V E) 14.0 V

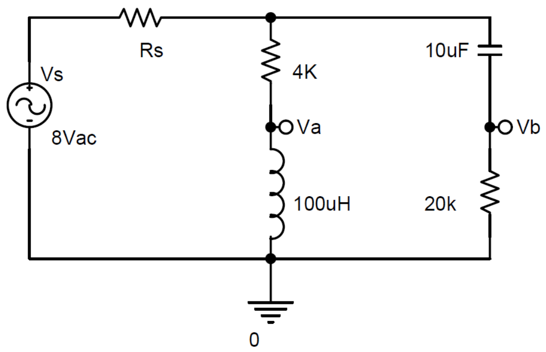
When the inductor is fully charged with the switch in position 1, it will have a current of Vs/(R1+R2) flowing through it to ground, or 14V/(120+820) Ω = 0.01489 A. When the switch is moved to 2, this current, Io = 0.01489 A will be flowing in the circuit and will decay in time with time constant T = L1/(R2+R3) = 0.1 H/(820+560)Ω = 72.5μs. After t=25μs the current will be I = Io*exp(-t/T) = 0.01489*exp(-25/75) = 0.01055 A. This current across R3 will give a voltage drop of 0.01055 A * 560 Ω = 5.91 V. Note that at the same time, the voltage across R2 will be 0.01055 A * 820 Ω = 8.65 V. Thus, the total voltage induced across the inductor will be 14.6 V due to the inductive kick of interrupting the circuit

8. If a sinusoidal voltage $v = V_p \sin \omega t$ is applied across a capacitor, C, what is the average value of the power dissipated in the capacitor?

A) 0 W B) CV_p^2 C) V_p^2/C D) $2CV_p^2$

Remember, no power is dissipated in reactive components.

9. For R_s= 10 kΩ, estimate the voltage V_b at very high frequencies.



A) 0 V　　**<u>B) 5 V</u>**　　C) 8 V　　D) One cannot estimate V_b.

At very high frequencies, capacitors look like wires ($X_C = 1/(\omega C) \rightarrow 0$) and inductors look like open circuits ($X_L = \omega L \rightarrow \infty$). So, make those approximations and one has an 8 V AC source across the series resistance R_s=10 kΩ + 20 kΩ in series (with no current flowing through the open branch with the 4 kΩ resistor). Current is 8 V/30 kΩ , and this is dropped across the 20 kΩ resistor, so V = 2/3*8 = 5.33 V.

10. At any resonant frequency in an RLC series circuit, what characteristics will the voltage across the two series reactive components have?

A) The applied voltage　　B) A reactive voltage
<u>C) There will be zero voltage</u>　　D) the same as the resistive voltage

The voltages in the L and C components will cancel out giving net 0 voltage across the two components.

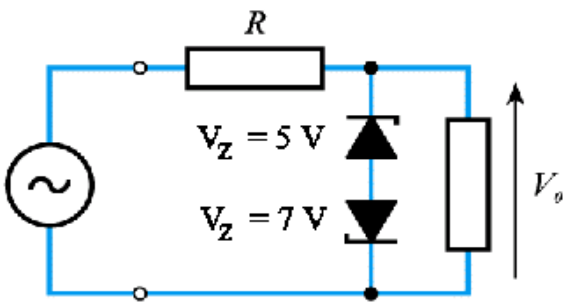
Multiple Choice Questions-2 (40% total).

There is only **one** correct answer so you must **choose the best answer**. Answer A, B, C, … (Capital letters). Correct answers give +4; incorrect or blank answers give 0.

Again, **on the answer sheet you turn in** use a table similar to the following:

Question	11	12	13	14	15	16	17	18	19	20
Answer	**C**	**A**	**A**	**C**	**B**	**A**	**E**	**D**	**A**	**C**

11. Estimate the maximum positive voltage produced by the following arrangement:



A) 7.7 V B) 6.3 V **C) 5.7 V** D) 4.3 V

During a positive cycle, the 5 V Zener diode is reversed biased and will breakdown when the voltage exceeds 5 V plus the internal voltage drop of the diode, ~0.7 V. The voltage cannot raise above that point, so the maximum positive voltage is 5.7 V.

12. An amplifier has a voltage gain of 20, an input resistance of 500 ohms and an output resistance of 50 ohms. The amplifier is connected to a voltage source that produces an output voltage of 1 V and has an output resistance of 75 ohms, and to a load resistance of 800 ohms. What is the voltage gain of this amplifier system?

A) **18.9 V**
B) 20 mV
C) 17.4 V
D) 16.4 V
E) 20 V
F) 0 V

Now both the input source and output of the amplifier can be loaded down. For example, the voltage source produces an output voltage of 1 V with an internal output resistance of 75 Ω, but this is in series with any load I place on it. Thus, R_o and R_L form a voltage divider so that the voltage that will actually appear across the load will be $V_s/(R_S+R_L)$ times R_L. In this case, the load is actually the input resistance of the amplifier, R_i, stated to be 500 Ω. Now, if this resistance were very much greater than the source output resistance, we could ignore the source output resistance and the voltage across the amplifier would be 1V. But here they are relatively similar, and the voltage across the input of the amplifier will be:

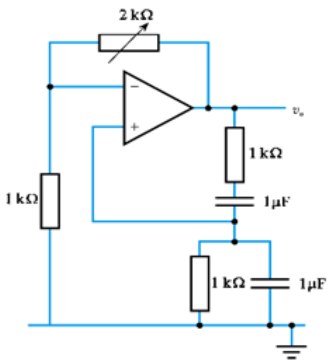
$V_s/(R_S+R_i)\cdot R_i = 1V/(575\Omega)\cdot 500\Omega = 0.870$ V.

Similarly, the amplifier will create a voltage $A_v \cdot V_i$, and drive this across an output impedance of 50 Ω. However, this is in series with the load resistor of 800 Ω. This means that the voltage that appears across this load is actually part of a voltage divider formed by R_o and R_L. So the voltage that appears across the load will be $A_v \cdot V_i/(R_o+R_L)$ times R_L. Now if R_L is very large compared to R_o, we can neglect R_o. Unfortunately here they are not so very different. The actual voltage across the load, the true output voltage of the amplifier, will be the divided voltage given above. This is:

$A_v \cdot V_i/(R_o+R_L) \cdot R_L = 20 \cdot 0.87V/(850\Omega) \cdot 800\Omega = 16.4\ V$

The effective gain of the amplifier is given by $V_o/V_i = 16.4/0.87 = 18.9$.

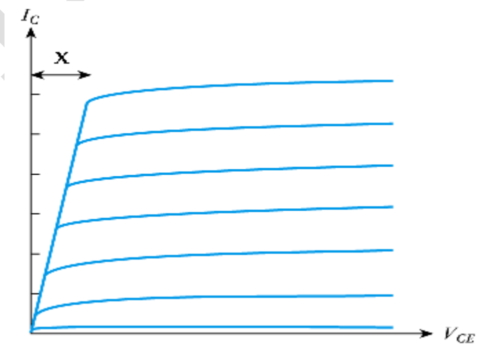
13. Calculate the frequency of oscillation of the Wien-bridge oscillator shown here.



<u>A) 159 Hz.</u> B) 238 Hz. C) 327 Hz. D) 424 Hz. E) 522 Hz.

One could do a non-trivial circuit analysis to get the equivalent frequency and phase shift. But again the better part of valour is to know the formula for the oscillation frequency $\omega = 1/(RC)$, and $f=\omega/(2\pi)$. So, $R=1000\Omega$ and $C = 1x10^{-6}F$ give $f = 159$ Hz

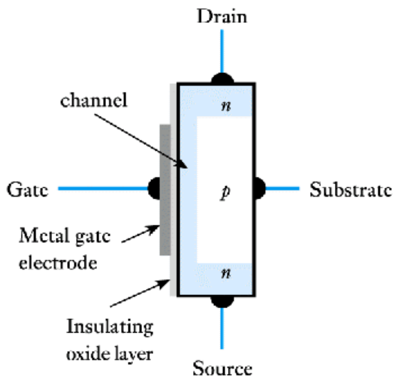
14. In the bipolar transistor output characteristics shown below, what region is represented by the symbol 'X'?



A) The active region
B) The space-charge region
C) <u>The saturation region</u>
D) The ohmic region

Here the region of the curve at low values of V_{CE} is called the saturation region. At these low values of V_{CE}, the transistor action does not occur and the transistor is in an "on" condition. This means that, assuming the base potential creates a forward bias between the base and emitter, there will also be a forward bias between the base and *the collector due to the small potential between the collector and emitter, V_{CE}. Under forward bias the depletion regions are physically very small, and a potential between the collector and the emitter drives the collector majority charge carriers into the base, where they recombine. However, it also drives the base majority charge into the emitter where they recombine. This represents a current between the collector and the emitter. This current will increase with V_{CE} until we reach a point where the collector becomes forward biased relative to the base, and transistor action can occur. Since both junctions are conducting and on, this is called saturation*

15. What form of FET is shown here?



A) An *n*-channel JFET.
B) An *n*-channel MOSFET.
C) A *p*-channel JFET.
D) A *p*-channel MOSFET.

The carrier channel from drain to source is an n-type material, and there is a metal oxide layer separating the gate from the channel. Thus, there is no current flow to the gate and answer A is correct.

16. What form of noise is produced as a result of the random, thermally induced motion of the atoms in a material?

A) **Johnson noise**.
B) Shot noise.
C) Flicker noise.
D) Interference.
E) Pink noise.

Definition of Johnson noise

17. Which logic gate has the following truth table?

A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

A) A two-input AND gate
B) A two-input EXCLUSIVE OR gate
C) A two-input NOR gate

D) A two-input EXCLUSIVE NOR gate
E) A two-input OR gate

Two input is clear since we have columns A and B. Next, we see that C is one if either A or B are 1, indicating an OR gate. The fact that A=1 at the same time that B=1 also produces C=1 is a characteristic of the OR gate. Whenever A = 1 includes the times when B is =1.

18. Simplify the expression $\boldsymbol{Y = (\overline{A+B}) \cdot (\overline{C+D+E}) + (\overline{A+B})}$:

A) $Y = A + B$
B) $Y = C + D + E$
C) $Y = \bar{C} \cdot \bar{D} \cdot \bar{E}$
D) $\underline{Y = \bar{A} \cdot \bar{B}}$
E) $Y = \bar{A} \cdot \bar{B} \cdot \bar{C} \cdot \bar{D} \cdot \bar{E}$
F) None of the above

By applying the property x + xy = x, with x = (A + B)'= A'B' and y = (C + D + E)'= C'D'E', we get the result.

19. What is the resolution of a 5-bit analogue (0-10V) to digital data converter?

A) 3% B) 6% C) 1.56% D) 10% E) 16%

Percentage resolution is the percentage of the full-scale output range that a change of 1 bit will give. Here, 5 bits will give 2^5=32 different output levels. So a change of 1 bit will give 5V / 32 = 0.156 V change. As a percentage of the full-scale output, 5 V, this is: (5V/32)/5V*100 = 1/32 * 100 = 3.125 %

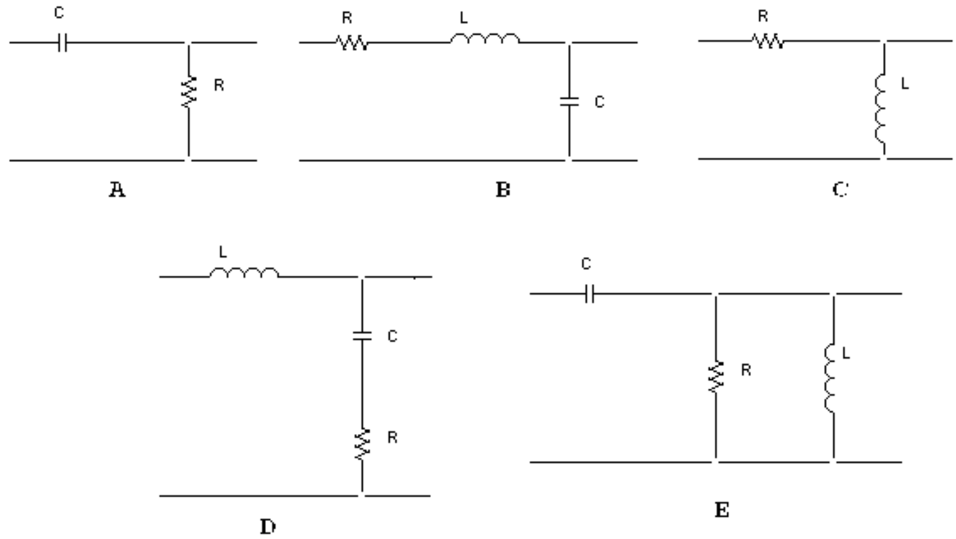
20. How many storage locations are available when a memory device has nine address lines?

A) 144 B) 256 C) 512 D) 2048 E) 4096

With 9 address lines, I can form a 9-bit binary number. With a 9 bit binary number, I can count from 0 to 511, or access 512 different locations (the address for the first location is 0).

Calculations (20% total)

21. **Shown below are 5 circuits. Assume that the input voltage (V_{in}) is applied across the leftmost terminals, and the output voltage, V_{out}, is measured across the rightmost terminals.**



Given below are several possible expressions for generic transfer functions for such circuits. Write down which function goes with which circuit. (2 points each)

$$\frac{j\omega L}{R + j\omega L + \frac{1}{j\omega C}}$$

A
$$\frac{R}{R + \frac{1}{j\omega C}}$$

D
$$\frac{R + \frac{1}{j\omega C}}{R + j\omega L + \frac{1}{j\omega C}}$$

$$\frac{j\omega C + \frac{1}{j\omega L}}{R + j\omega C + \frac{1}{j\omega L}}$$

B
$$\frac{\frac{1}{j\omega C}}{R + j\omega L + \frac{1}{j\omega C}}$$

$$\frac{R}{R + j\omega L}$$

C
$$\frac{j\omega L}{R + j\omega L}$$

$$\frac{R + j\omega L}{R + j\omega L + \frac{1}{j\omega C}}$$

$$\frac{\frac{R}{j\omega RC + 1}}{j\omega L + \frac{R}{j\omega RC + 1}}$$

$$\frac{R}{R + j\omega L + \frac{1}{j\omega C}}$$

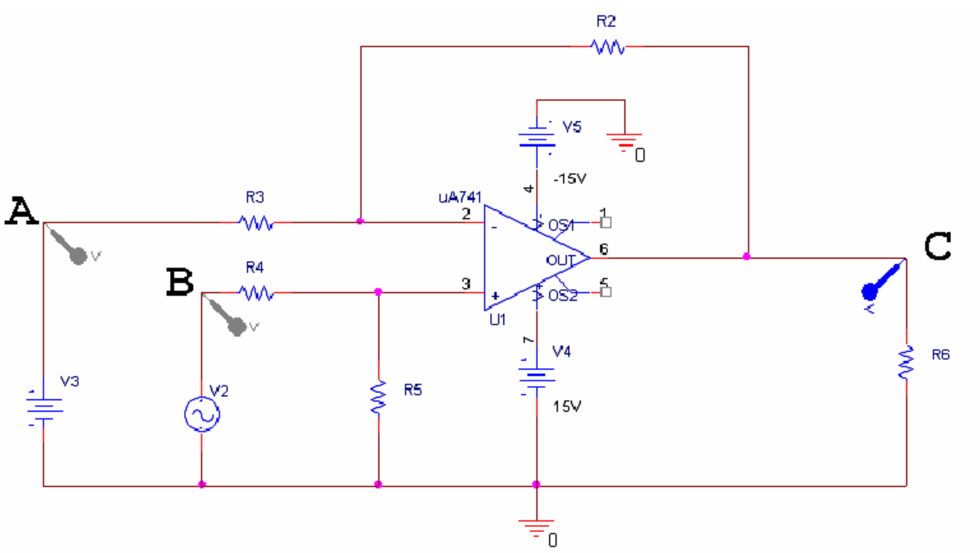
$$\frac{\frac{1}{j\omega C}}{R + \frac{1}{j\omega C}}$$

$$\frac{j\omega L + \frac{1}{j\omega C}}{R + j\omega L + \frac{1}{j\omega C}}$$

E
$$\frac{\frac{j\omega LR}{R + j\omega L}}{\frac{1}{j\omega C} + \frac{j\omega LR}{R + j\omega L}}$$

22. For the circuit below, assume the following about the components:

> **V2: has a DC offset of 500mV, and an AC amplitude 100 mV at a frequency of 1 KHz**
>
> **V3: is a DC voltage of 300mV**
>
> **R2=18 kΩ, R3=3 kΩ, R4=3 kΩ, R5=18 kΩ, R6=10 kΩ**



a. **What kind of amplifier is this (1%)**
   Difference (or differential) amplifier

b. **Write an expression for the input signal at B in the form $v(t)=A\sin(\omega t) + V_{DC}$, using the values above (3%)**
   $v(t) = 200\text{mV} \sin(2\cdot 1000\,\pi\ t) + 600\text{ mV}$

c. **Write an equation for the output at C (V_C) in terms of the input voltages V2 and V3. Simplify, but do not substitute for V2 and V3. (2%)**
   $Vc = [10K/2K]\,(V2 - V3) = 5(V2-V3)$

d. **Write an expression for the output signal at C in the form $v(t)=A\sin(\omega t) + V_{DC}$ substituting in values. (4%)**

   $Vc = 5\,[200\text{mV} \sin(2\cdot 1000\,\pi\ t) + 600\text{ mV} - 200\text{ mV}]$
   $Vc = 1000\text{mV} \sin(2000\,\pi\ t) + 2000\text{ mV}$
   $Vc = 1\text{V} \sin(2000\,\pi\ t) + 2\text{V}$

BJT parameters for common emitter configuration (subscript $_e$)

other subscripts: Input$_i$ Output$_o$ Forward$_f$ Reverse$_r$

h_{FE}	DC gain	I_C / I_B	
h_{fe}	AC gain	i_c / i_b	$h_{FE} \approx h_{fe}$ (mostly)
g_m	Transconductance	$\Delta I_C / \Delta V_{BE} = i_c / v_{be}$	$\sim 40 \cdot I_C \approx 40 \cdot I_E$
h_{ie}	Small signal input resistance	$\Delta V_{BE} / \Delta I_B = v_{be} / i_b$	$\sim 1 / (40 \cdot I_B)\ \Omega \approx h_{fe} / (40 \cdot I_C)$
h_{oe}	Output admittance ($1/r_o$) where r_o = Slope in the active region	$\Delta I_C / \Delta V_{CE} = i_c / v_{ce}$	
r_e	Emitter resistance	$\Delta V_{BE} / \Delta I_C = v_{be} / i_c = 1/g_m$	$\approx v_{be} / i_e$ that is, $h_{ie} = h_{fe} \cdot r_e$
h_{re}	Early effect (V_{CE} affects bias V_{BE})	$\Delta V_{CE} / \Delta V_{BE}$	

$$h_{FE} = \frac{I_C}{I_B}$$

$$I_E = I_C + I_B = (h_{FE} + 1) \cdot I_B$$

$$\text{but because } h_{FE} >> 1,$$

$$I_E \approx h_{FE} \cdot I_B = I_C$$

$$I_B = I_{BS} \cdot e^{40 \cdot V_{BE}} \quad \text{where } I_{BS} \text{ is constant}$$

$$I_C = h_{FE} \cdot I_B = h_{FE} \cdot I_{BS} \cdot e^{40 \cdot V_{BE}}$$

$$g_m = \frac{\Delta I_C}{\Delta V_{BE}} = \frac{dI_C}{dV_{BE}} = 40 \cdot h_{FE} \cdot I_{BS} \cdot e^{40 \cdot V_{BE}}$$

$$g_m = \qquad = 40 \cdot I_C \approx 40 \cdot I_E$$